

## CD4066BC Quad Bilateral Switch

### General Description

The CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

### Features

- Wide supply voltage range 3V to 15V
- High noise immunity 0.45  $V_{DD}$  (typ.)
- Wide range of digital and analog switching  $\pm 7.5 V_{PEAK}$
- "ON" resistance for 15V operation 80 $\Omega$
- Matched "ON" resistance  $\Delta R_{ON}=5\Omega$  (typ.) over 15V signal input
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio @  $f_{is} = 10$  kHz,  $R_L = 10$  k $\Omega$
- High degree linearity 0.1% distortion (typ.)
- High degree linearity @  $f_{is} = 1$  kHz,  $V_{is} = 5V_{p-p}$

- High degree linearity  $V_{DD}-V_{SS} = 10V$ ,  $R_L = 10$  k $\Omega$
- Extremely low "OFF" switch leakage: @  $V_{DD}-V_{SS} = 10V$ ,  $T_A = 25^\circ C$  0.1 nA (typ.)
- Extremely high control input impedance 10<sup>12</sup> $\Omega$ (typ.)
- Low crosstalk -50 dB (typ.) between switches @  $f_{is} = 0.9$  MHz,  $R_L = 1$  k $\Omega$
- Frequency response, switch "ON" 40 MHz (typ.)

### Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

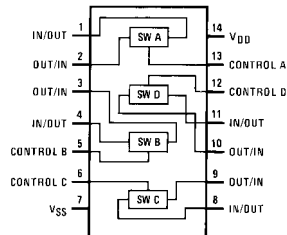
### Ordering Code:

Order Number	Package Number	Package Description
CD4066BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
CD4066BCJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4066BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

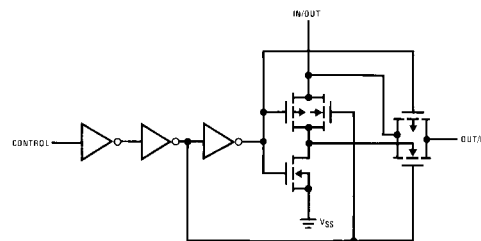
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

### Connection Diagram

Pin Assignments for SOIC, SOP and DIP



### Schematic Diagram



**Absolute Maximum Ratings**

(Note 1)

(Note 2)

Supply Voltage ( $V_{DD}$ )	-0.5V to +18V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{CC}+0.5V$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	300°C

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{DD}$ )	3V to 15V
Input Voltage ( $V_{IN}$ )	0V to $V_{DD}$
Operating Temperature Range ( $T_A$ )	-40°C to +85°C

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

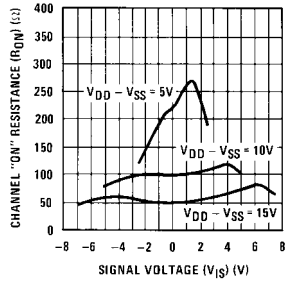
**DC Electrical Characteristics** (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V$		1.0		0.01	1.0		7.5	$\mu A$
		$V_{DD} = 10V$		2.0		0.01	2.0		15	$\mu A$
		$V_{DD} = 15V$		4.0		0.01	4.0		30	$\mu A$
<b>SIGNAL INPUTS AND OUTPUTS</b>										
$R_{ON}$	"ON" Resistance	$R_L = 10\text{ k}\Omega$ to $(V_{DD} - V_{SS}/2)$ $V_C = V_{DD}, V_{SS}$ to $V_{DD}$								
		$V_{DD} = 5V$		850		270	1050		1200	$\Omega$
		$V_{DD} = 10V$		330		120	400		520	$\Omega$
		$V_{DD} = 15V$		210		80	240		300	$\Omega$
$\Delta R_{ON}$	$\Delta$ "ON" Resistance Between Any 2 of 4 Switches	$R_L = 10\text{ k}\Omega$ to $(V_{DD} - V_{SS}/2)$ $V_{CC} = V_{DD}, V_{IS} = V_{SS}$ to $V_{DD}$								
		$V_{DD} = 10V$				10				$\Omega$
		$V_{DD} = 15V$				5				$\Omega$
$I_{IS}$	Input or Output Leakage Switch "OFF"	$V_C = 0$		$\pm 50$		$\pm 0.1$	$\pm 50$		$\pm 200$	nA
<b>CONTROL INPUTS</b>										
$V_{ILC}$	LOW Level Input Voltage	$V_{IS} = V_{SS}$ and $V_{DD}$ $V_{OS} = V_{DD}$ and $V_{SS}$ $I_{IS} = \pm 10\mu A$								
		$V_{DD} = 5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$		4.0		6.75	4.0		4.0	V
$V_{IHC}$	HIGH Level Input Voltage	$V_{DD} = 5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$ (Note 7)	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$	11.0		11.0	8.25		11.0		V
$I_{IN}$	Input Current	$V_{DD} - V_{SS} = 15V$ $V_{DD} \geq V_{IS} \geq V_{SS}$ $V_{DD} \geq V_C \geq V_{SS}$		$\pm 0.3$		$\pm 10^{-5}$	$\pm 0.3$		$\pm 1.0$	$\mu A$

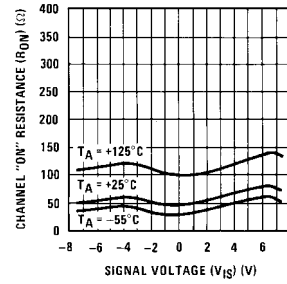
<b>AC Electrical Characteristics</b> (Note 3)						
$T_A = 25^\circ\text{C}$ , $t_r = t_f = 20\text{ ns}$ and $V_{SS} = 0\text{V}$ unless otherwise noted						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PHL}$ , $t_{PLH}$	Propagation Delay Time Signal Input to Signal Output	$V_C = V_{DD}$ , $C_L = 50\text{ pF}$ , (Figure 1)				
		$R_L = 200\text{ k}$				
		$V_{DD} = 5\text{V}$		25	55	ns
		$V_{DD} = 10\text{V}$		15	35	ns
		$V_{DD} = 15\text{V}$		10	25	ns
$t_{PZH}$ , $t_{PZL}$	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$R_L = 1.0\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , (Figure 2, Figure 3)				
		$V_{DD} = 5\text{V}$			125	ns
		$V_{DD} = 10\text{V}$			60	ns
		$V_{DD} = 15\text{V}$			50	ns
$t_{PHZ}$ , $t_{PLZ}$	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance Sine Wave Distortion  Frequency Response-Switch "ON" (Frequency at -3 dB)	$R_L = 1.0\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , (Figure 2, Figure 3)				
		$V_{DD} = 5\text{V}$			125	ns
		$V_{DD} = 10\text{V}$			60	ns
		$V_{DD} = 15\text{V}$			50	ns
		$V_C = V_{DD} = 5\text{V}$ , $V_{SS} = -5\text{V}$ $R_L = 10\text{ k}\Omega$ , $V_{IS} = 5V_{p-p}$ , $f = 1\text{ kHz}$ , (Figure 4)	0.1			%
	$V_C = V_{DD} = 5\text{V}$ , $V_{SS} = -5\text{V}$ , $R_L = 1\text{ k}\Omega$ , $V_{IS} = 5V_{p-p}$ , $20\text{ Log}_{10} V_{OS}/V_{OS}$ (1 kHz)-dB, (Figure 4)	40			MHz	
	Feedthrough — Switch "OFF" (Frequency at -50 dB)  Crosstalk Between Any Two Switches (Frequency at -50 dB)  Crosstalk; Control Input to Signal Output  Maximum Control Input	$V_{DD} = 5.0\text{V}$ , $V_{CC} = V_{SS} = -5.0\text{V}$ , $R_L = 1\text{ k}\Omega$ , $V_{IS} = 5.0V_{p-p}$ , $20\text{ Log}_{10}$ , $V_{OS}/V_{IS} = -50\text{ dB}$ , (Figure 4)		1.25		
		$V_{DD} = V_{C(A)} = 5.0\text{V}$ ; $V_{SS} = V_{C(B)} = 5.0\text{V}$ , $R_L = 1\text{ k}\Omega$ , $V_{IS(A)} = 5.0V_{p-p}$ , $20\text{ Log}_{10}$ , $V_{OS(B)}/V_{IS(A)} = -50\text{ dB}$ (Figure 5)		0.9		MHz
		$V_{DD} = 10\text{V}$ , $R_L = 10\text{ k}\Omega$ , $R_{IN} = 1.0\text{ k}\Omega$ , $V_{CC} = 10\text{V}$ Square Wave, $C_L = 50\text{ pF}$ (Figure 6)		150		mV <sub>p-p</sub>
		$R_L = 1.0\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , (Figure 7) $V_{OS(f)} = \frac{1}{2} V_{OS}(1.0\text{ kHz})$		6.0		MHz
		$V_{DD} = 5.0\text{V}$		8.0		MHz
		$V_{DD} = 10\text{V}$		8.5	MHz	
		$V_{DD} = 15\text{V}$				
$C_{IS}$	Signal Input Capacitance			8.0		pF
$C_{OS}$	Signal Output Capacitance	$V_{DD} = 10\text{V}$		8.0		pF
$C_{IOS}$	Feedthrough Capacitance	$V_C = 0\text{V}$		0.5		pF
$C_{IN}$	Control Input Capacitance			5.0	7.5	pF
<b>Note 3:</b> AC Parameters are guaranteed by DC correlated testing.						
<b>Note 4:</b> These devices should not be connected to circuits with the power "ON".						
<b>Note 5:</b> In all cases, there is approximately 5 pF of probe and jig capacitance in the output; however, this capacitance is included in $C_L$ wherever it is specified.						
<b>Note 6:</b> $V_{IS}$ is the voltage at the in/out pin and $V_{OS}$ is the voltage at the out/in pin. $V_C$ is the voltage at the control input.						
<b>Note 7:</b> Conditions for $V_{IHC}$ : a) $V_{IS} = V_{DD}$ , $I_{OS} = \text{standard B series } I_{OH}$ b) $V_{IS} = 0\text{V}$ , $I_{OL} = \text{standard B series } I_{OL}$ .						

## Typical Performance Characteristics

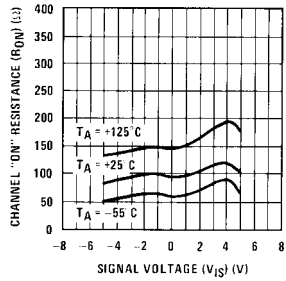
“ON” Resistance vs Signal Voltage for  $T_A = 25^\circ\text{C}$



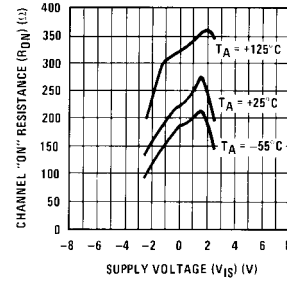
“ON” Resistance as a Function of Temperature for  $V_{DD} - V_{SS} = 15\text{V}$



“ON” Resistance as a Function of Temperature for  $V_{DD} - V_{SS} = 10\text{V}$



“ON” Resistance as a Function of Temperature for  $V_{DD} - V_{SS} = 5\text{V}$



## Special Considerations

In applications where separate power sources are used to drive  $V_{DD}$  and the signal input, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$  = effective external load of the 4 CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action of the  $V_{DD}$  supply when power is applied or removed from CD4066BC.

In certain applications, the external load-resistor current may include both  $V_{DD}$  and signal-line components. To

avoid drawing  $V_{DD}$  current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at  $T_A \leq 25^\circ\text{C}$ , or 0.4V at  $T_A > 25^\circ\text{C}$  (calculated from  $R_{ON}$  values shown).

No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminals 2, 3, 9 or 10.

AC Test Circuits and Switching Time Waveforms

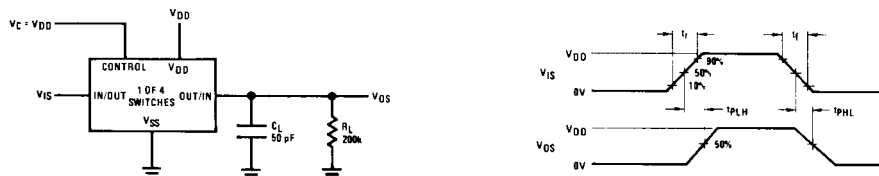


FIGURE 1.  $t_{PHL}$ ,  $t_{PLH}$  Propagation Delay Time Signal Input to Signal Output

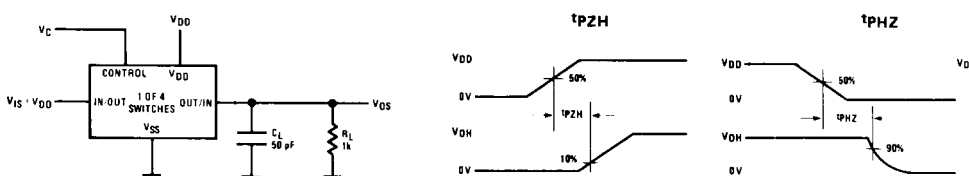


FIGURE 2.  $t_{PZH}$ ,  $t_{PHZ}$  Propagation Delay Time Control to Signal Output

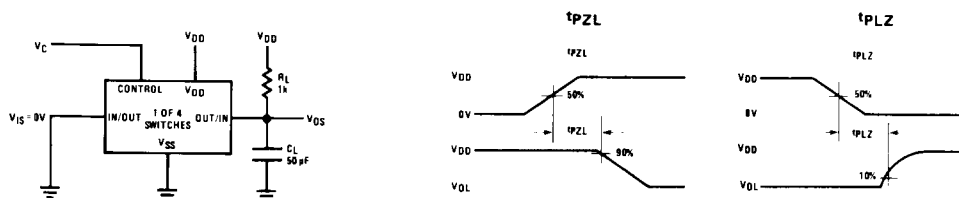
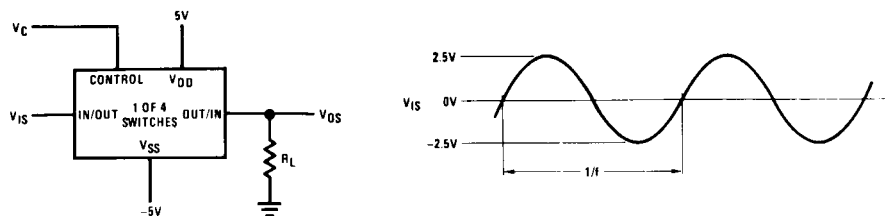


FIGURE 3.  $t_{PZL}$ ,  $t_{PLZ}$  Propagation Delay Time Control to Signal Output



$V_C = V_{DD}$  for distortion and frequency response tests

$V_C = V_{SS}$  for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

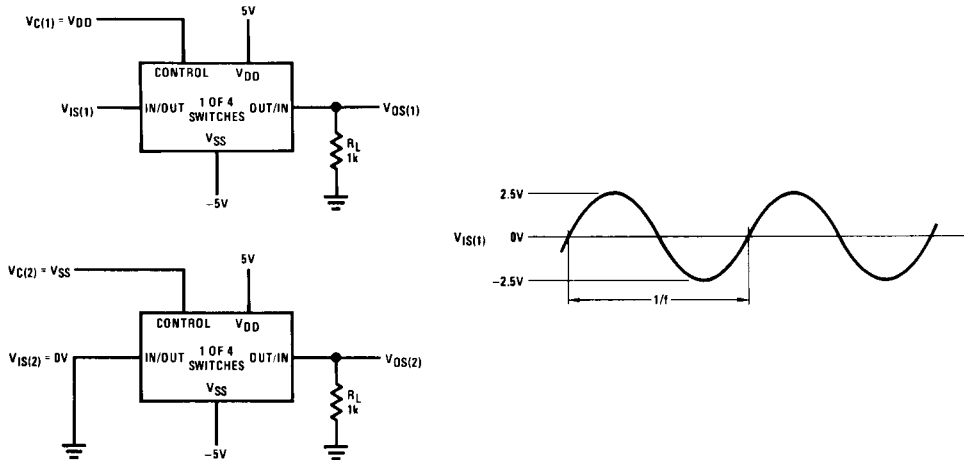


FIGURE 5. Crosstalk Between Any Two Switches

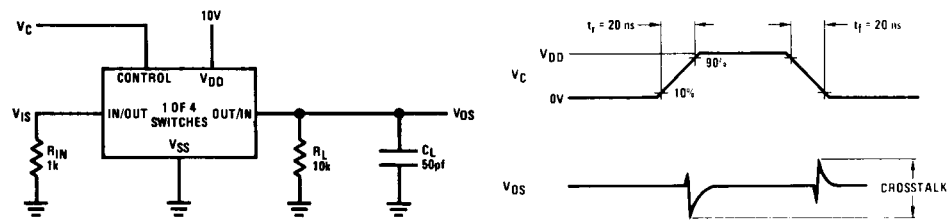


FIGURE 6. Crosstalk: Control Input to Signal Output

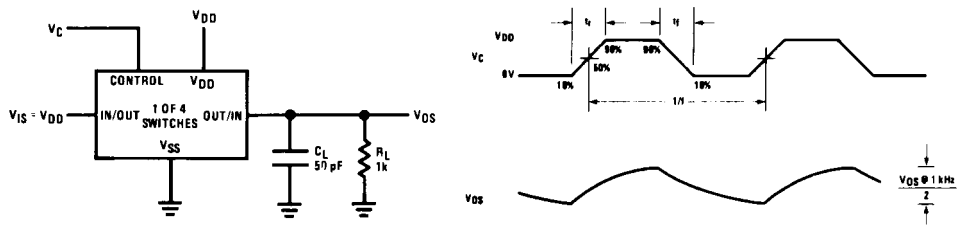
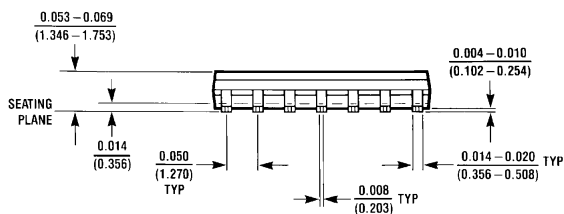
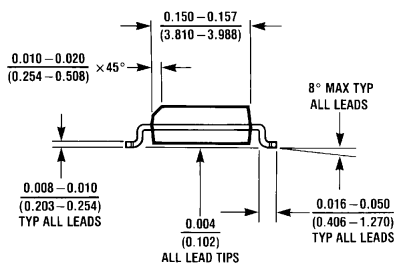
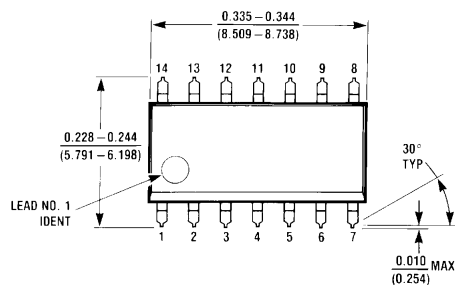


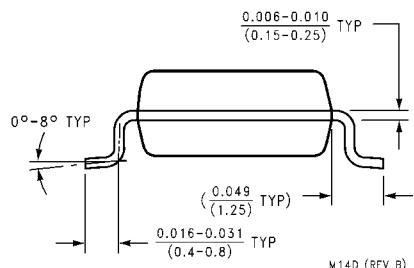
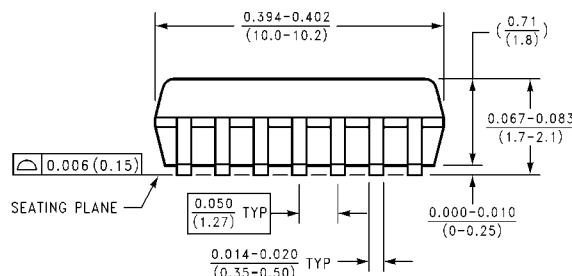
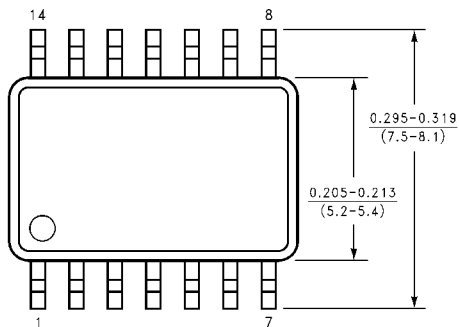
FIGURE 7. Maximum Control Input Frequency

**Physical Dimensions** inches (millimeters) unless otherwise noted



M14A (REV H)

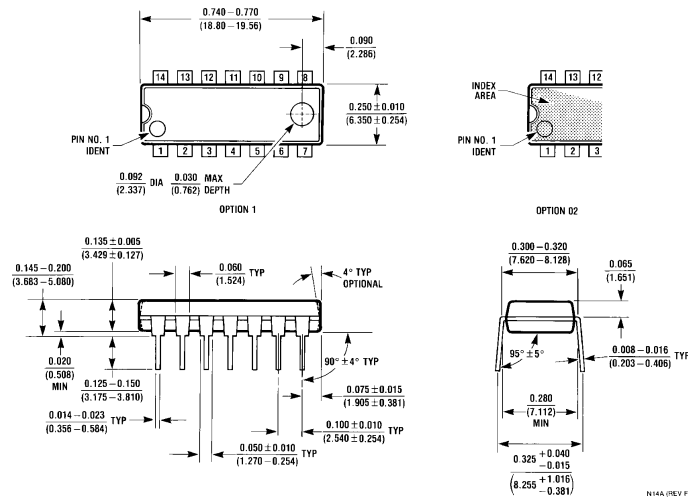
**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body  
Package Number M14A**



M14D (REV B)

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A**

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